In the Abstract

Please amend the ABSTRACT OF THE DISCLOSURE of this application as follows:

A1

--A data processing system with a microprocessor ~~(10)~~. The microprocessor has in instruction execution pipeline includes fetch and decode stages and several functional execution units ~~(L1/2, S1/2, M1/2, D1/2)~~. Fetch packets ~~(700, 702, 704)~~ contain a plurality of instruction words. ~~Execution~~ Execute packets ~~(EP1 … EP5)~~ include a plurality of instruction words that can be executed in parallel by two or more execution units. An execution packet can span two or more fetch packets. A predetermined bit in each instruction marks whether the next instruction is executed in parallel with the current instruction. Instructions in an execute packet are dispatched to appropriate functional execution units based on instruction type. Upon a branch into an execute packet instructions at memory addresses before the branch location are not executed in parallel with instructions following the branch location.

~~Figure 7B~~--